ROHDE&SCHWARZ

USER MANUAL

Digital Function Test Module

TS-PDFT

User Manual

for ROHDE & SCHWARZ Digital Function Test Module TS-PDFT

4th Issue / 11.05 / GB 1152.3820.12

ROHDE & SCHWARZ GmbH & Co. KG
Corporate Headquarters
Mühldorfstr. 15
D-81671 München

Telephone: ...49 (0)89/4129-13774
Fax: ...49 (0)89/4129-13777

Printed in the Federal Republic of Germany. Errors excepted, subject to technical change without notice.

Safety Instructions

Attention!
Electrostatic sensitive devices require special care

CERTIFICATE

DQS GmbH

Deutsche Gesellschaft zur Zertifizierung von Managementsystemen

hereby certifies that the company

Rohde & Schwarz GmbH & Co. KG

Mühldorfstrasse 15
D-81671 München

with the production sites as listed in the annex

for the scope
Design and Development, Production, Sales, Services of Electronic-Measurement and Communication-Equipment and Systems

has implemented and maintains a

Quality Management System.

An audit, documented in a report, has verified that this quality management system fulfills the requirements of the following standard:

DIN EN ISO 9001 : 2000

December 2000 edition

The quality management system of the sites marked with (*) in the annex fulfills the requirements set out by the international and German Road Traffic Regulations
including the approval objects as listed in the appendix.

This certificate is valid until	2008-01-23
Certificate Registration No.	001954 QM/ST
Frankfurt am Main	2005-01-24

This certificate is based on a quality audit in cooperation with the CETECOM ICT Services GmbH as a Notified Body under the Scope of the EC directive 99/5/EC.
It was verified by the Notified Body that the supplementary requirements of the Annex V of the European Concil Directive 99/5/EC are fulfilled.

Ass. iur. M. Drechsel
Dipl.-Ing. S. Heinloth
MANAGING DIRECTORS

Senior Executive Officer of CETECOM ICT Services GmbH
Dipl.-Ing. J. Schirra

DQS is member of: IQNet THE INTERNATIONAL CERTIFICATION NETWORK

D-60433 Frankfurt am Main, August-Schanz-Straße 21

Deutscher Akkreditierungs Rat DAR
TGA-ZM-02-90
KBA-ZM-A 00023-95

Appendix to Certificate Registration No.: 001954 QM/ST

Rohde & Schwarz GmbH & Co. KG

Mühldorfstrasse 15
D-81671 München

The international and German Road Traffic Law
was audited regarding the following approval objects:

No.: 22 Electrical/Electronic Sub Assembly

This appendix (as of 2005-01-24) is only valid in connection
with the above-mentioned certificate.

Annex to Certificate Registration No.: 001954 QM ST

Rohde & Schwarz GmbH & Co. KG

Mühldorfstrasse 15
D-81671 München

Organizational unit/site	Scope
ROHDE & SCHWARZ GmbH & Co. KG Service Centre Cologne **ROHDE & SCHWARZ Systems GmbH** Graf-Zeppelin-Strasse 18 D-51147 Köln	Technical services in the field of measuring/communication techniques maintenance/repair calibration training technical documentation Development, production, systems
Rohde & Schwarz FTK GmbH Wendenschloßstrasse 168 D-12557 Berlin	Design and Development, Production and Sale of Communication Equipment, Installations and systems
Rohde & Schwarz GmbH & Co. KG Kaikenrieder Strasse 27 D-94244 Teisnach	Design and Development, Production, Sales, Services of Electronic-Measurement and Communication-Equipment and Systems
Rohde & Schwarz závod Vimperk s.r.o. Spidrova 49 CZE-38501 Vimperk Tschechische Republik	Design and Development, Production, Sales, Services of Electronic-Measurement and Communication-Equipment and Systems
(*) **Rohde & Schwarz GmbH & Co. KG** Mühldorfstrasse 15 81671 München	Design and Development, Production, Sales, Services of Electronic-Measurement and Communication-Equipment and Systems
(*) **Rohde & Schwarz Messgerätebau GmbH** Riedbachstrasse 58 D-87700 Memmingen	Design and Development, Production, Sales, Services of Electronic-Measurement and Communication-Equipment and Systems

This annex (as of 2005-01-24)is only valid in connection with the above-mentioned certificate.

Support Center

Telephone Europe: **+49 180 512 42 42**

Telephone worldwide: **+49 89 4129 13774**

Fax: **+49 89 4129 13777**

e-mail: customersupport@rohde-schwarz.com

If you have any technical queries about this Rohde & Schwarz equipment, our Hotline at the Support Center of Rohde & Schwarz Sales-GmbH will be glad to help.

Our team will discuss your queries and look for solutions to your problems.

The Hotline is open Mondays to Fridays from 08.00 to 17.00 hrs.

For queries outside office hours, you can leave a message or send a note via fax or email. We will then get back to you as soon as possible.

ROHDE & SCHWARZ

Content

4th Issue 11.05

4th Issue 11.05

Figures

4th Issue 11.05

4th Issue 11.05

Tables

4th Issue 11.05

4th Issue 11.05

1 Usage

1.1 General

The ROHDE & SCHWARZ Digital Function Test Module TS-PDFT is ideal for use wherever simple or complex digital circuits are tested or programmed by static or dynamic stimulation/recording/communication. The deterministic simultaneous stimulation/recording of digital signals makes it possible to simulate test scenarios under near-actual conditions. A local microprocessor ensures high computing power with time-critical communication protocols, downloads of flash memories or analyses directly on the module. Comprehensive trigger options with pattern comparators or the PXI Triggerbus allow synchronization with other R&S measurement, stimulus or switching modules or PXI modules of other manufacturers.

A LabWindows IVI driver is provided on the module for the general functions. All other hardware functions are controlled using specific extensions of the driver. As is typical for a LabWindows CVI driver, Function Panels and Online Help are available.

The TS-PDFT module is inserted in the front of the CompactTSVP chassis. It is based on the cPCI/PXI standard.

The TS-PDFT module can only be used in the CompactTSVP (TSVP = Test System Versatile Platform).

4th Issue 11.05

1.2 Characteristics

The TS-PDFT Digital Function Test Module features the following characteristics:

Characteristics TS-PDFT
64-channel digital function test card (32x IN, 32x OUT)
Simultaneous clocked pattern generating/recording (max. 40 MS/s)
An output level range (0 ... +10 V) that can be programmed in groups
A high output current (max. 150 mA/channel, 500 mA/group), short-circuit resistant
Input threshold voltage/hysteresis (0 ... 38 V) that can be programmed in groups
Serial comm ports (CAN, K-Bus, RS232)
Local microprocessor
Synchronization by PXI Triggerbus
Self-test capability
Used in the *CompactTSVP*

Table 1-1 Characteristics TS-PDFT

1.2.1 Applications

The TS-PDFT function test module is used to test the operation of digitally mounted modules or devices. Function tests of this type test the entire operation of a digital circuit under conditions that are as near to reality as possible. The module does this by creating digital input patterns, measuring the output signals and comparing them with the target values.

The following applications are available with the TS-PDFT digital function test module:

- Digital function test (Low-Speed/High-Speed)
- Bit pattern stimulation (Low-Speed/High-Speed)
- Bit pattern measuring (Low-Speed/High-Speed)
- Monitoring of level state changes (pattern trigger)
- Digital function test at component level (no node forcing, backdriving capability)
- Protocol analysis/generation (CAN, K-Bus, RS232)

4th Issue 11.05

- Downloads, e.g. for flash components, serial and parallel

A typical function test will comprise the following tasks:

- **Adapting the pin electronics to the environment of the unit under test (logic level and logic family)**
- **Defining the sensor strobe**
- **Defining the stimulus and measuring response of the module pins (PDFT)**
- **Evaluating the test results**

Should the application require additional digital channels, this can be achieved by cascading further TS-PDFT function test modules and synchronizing them with the PXI Triggerbus. The ability to program the modes, output levels and input threshold values in groups makes for an optimum adaption to the requirements of the application. Power relays and pulse-width modulable power outputs further complement the functionality. Serial communications interfaces such as CAN High/Low-Speed, K-Bus and RS232 are controlled by a powerful local microprocessor. Downloadable firmware applets can also be used to create application-specific interface protocols.

The extremely compact design with I/O suppressor circuitry and signal conditioning occupies just a single Compact PCI/PXI slot width, making it possible to create space-saving yet very powerful measurement and stimulus systems.

The hysteresis of the input channels can be programmed to minimize electrical transients. The lower and upper threshold voltages can be set separately in groups. The robustness of the TS-PDFT function test module is further enhanced by suppressor circuits that prevent shorts, back-e.m.f. and overvoltage.

The TS-PDFT function test module can perform a full self-test without any additional measurement effort. Diagnostic LEDs in the front panel indicate the module's status.

4th Issue 11.05

1.2.2 Digital Function Test

1.2.2.1 Digital Function Test (Low-Speed)

The digital function test (Low-Speed) tests functionalities where the emphasis is more on the correct interplay of logic chips and less on proving time-critical limits. The application lays down the patterns that must be stimulated and the expected responses. A comparison of the two targets produces a PASS/FAIL outcome. Other applications include the testing / stimulating of digital interfaces and downloading data into a programmable chip within the circuit.

1.2.2.2 Digital Function Test (High-Speed)

The real-time test tests the complete function of the digital part of a UUT under operating conditions that are as near to reality as possible. This is done by applying digital patterns (vectors) with a high clock-pulse rate and accurate time response to the UUT's connections and recording its reactions. For exact and predictable timing it is essential that the patterns are stored in pin memories behind the driver sensors and are processed at high speed (dynamic channels). The same is true for recording the test results and errors for subsequent evaluation and analysis.

4th Issue 11.05

2 View

Figure 2-1 shows the TS-PDFT Function Test Module

Figure 2-1 View of the TS-PDFT module

4th Issue 11.05

4th Issue 11.05

3 Block Diagrams

This section provides a function chart of the TS-PDFT module as well as a detailed block diagram.

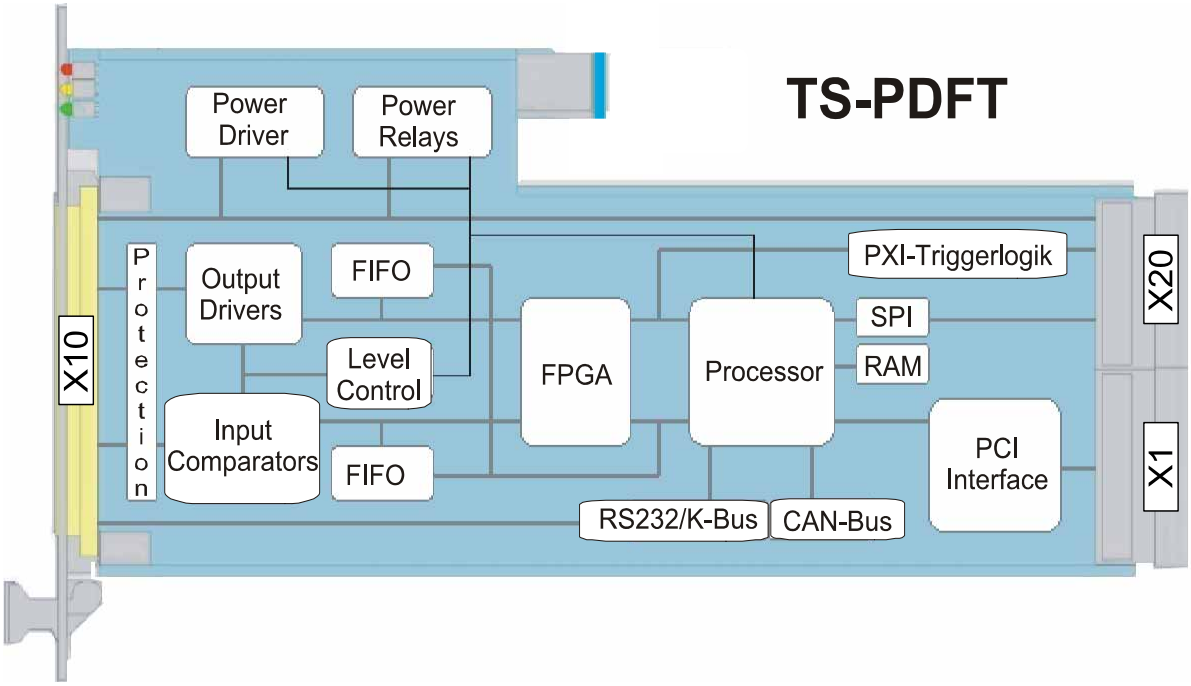

Figure 3-1 Function chart of the TS-PDFT module

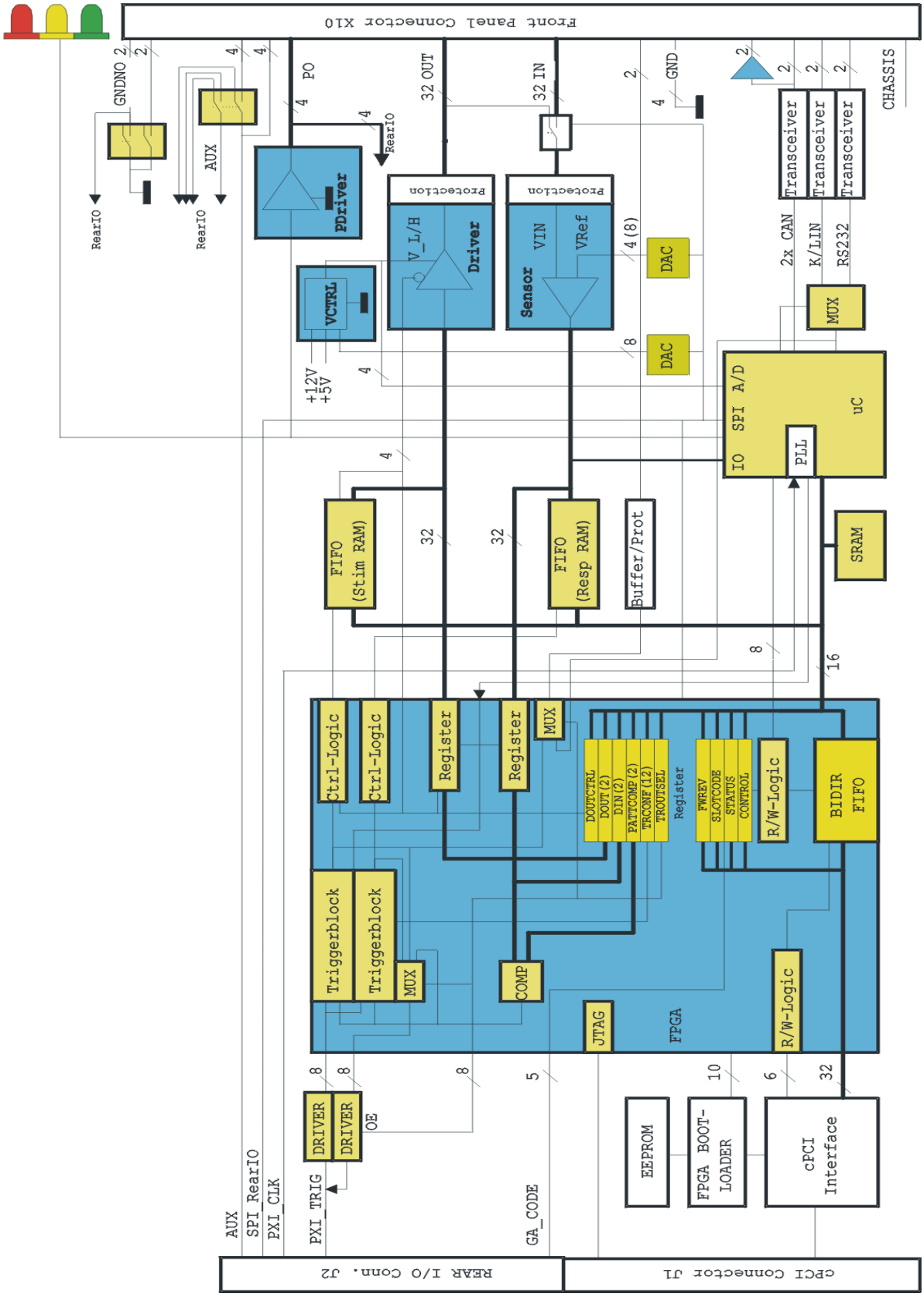

Figure 3-2 Detailed block diagram of the TS-PDFT module

4th Issue 11.05

4 Layout

4.1 Mechanical Layout

The TS-PDFT module is designed as a **long cPCI plug-in module** for mounting in the front of the CompactTSVP. The board height of the module is 3 HU (134 mm). The front panel is provided with a locating pin to ensure that it is correctly inserted into the Compact TSVP. The module is locked in place with the two retaining screws on the front panel. Front connector X10 is used for connecting the UUTs. X20/X1 connectors connect the TS-PDFT module to the cPCI backplane/PXI control backplane. The X50 connector is prepared for an optional push-on module.

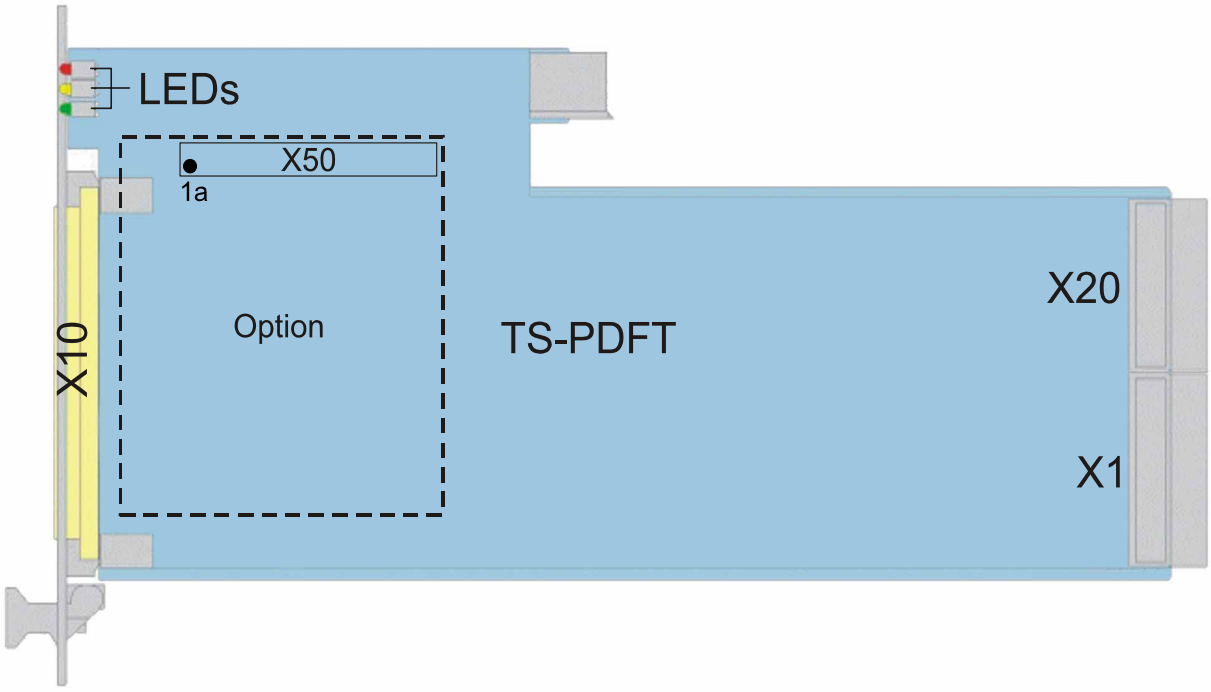

Figure 4-1 Layout of the connectors on the TS-PDFT module

Symbol	Use
X1	cPCI Bus
X10	Unit Under Test (UUT)
X20	Extension (PXI), Rear I/O
X50	Optional push-on module

Table 4-1 Connectors of the TS-PDFT module

4.1.1 Display elements of the TS-PDFT Module

Three light-emitting diodes (LEDs) on the front of the TS-PDFT module indicate its current status. These LEDs have the following meanings:

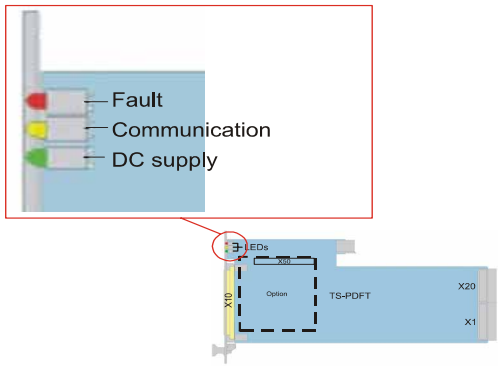

Figure 4-2 Layout of the LEDs on the TS-PDFT module

LED	Description
red	Fault (ERR): Lights up when a fault is detected on the TS-PDFT module during the power-on test after the supply voltage is switched on. This indicates the presence of a hardware problem on the module. (see also Section 8 “Self-Test“)
yellow	Communication (COM): Lights up when data is exchanged across the interface.
green	Supply voltage OK (PWR): Lights up when all the necessary supply voltages are present.

Table 4-2 Display elements on the TS-PDFT module

5 Function Description

See also Figures 5-1 to 5-4

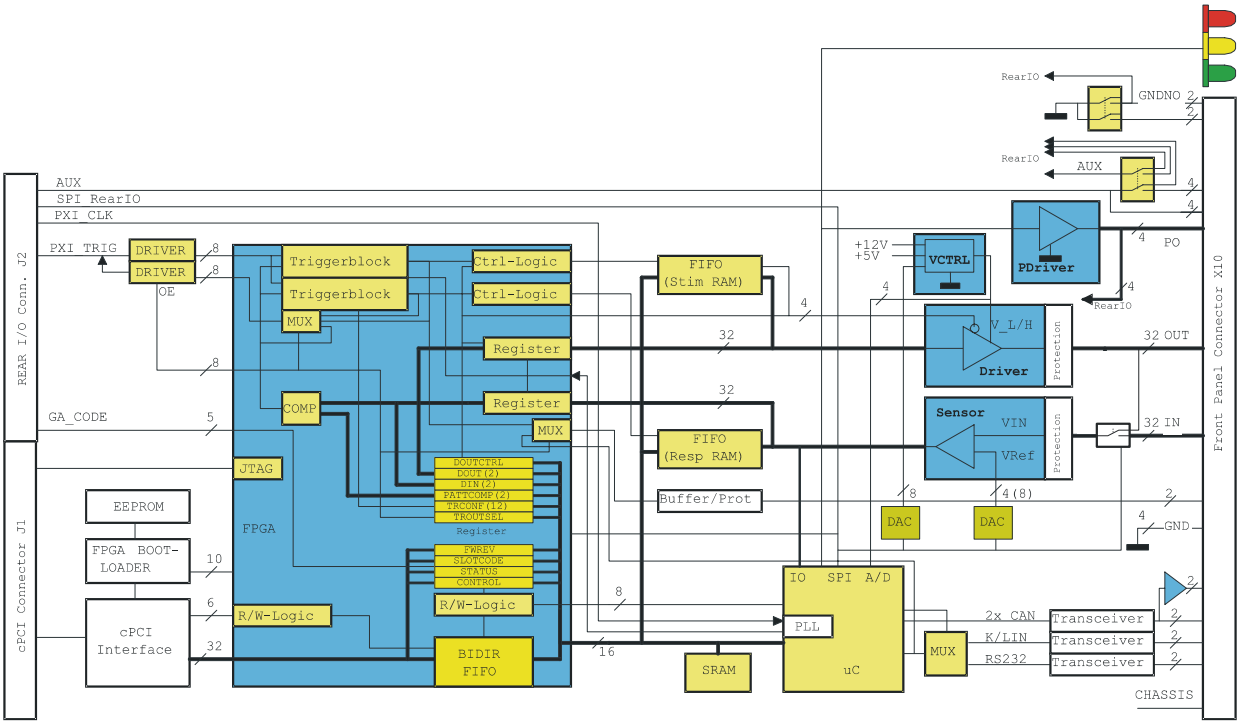

Figure 5-1 Block diagram of the TS-PDFT module

5.1 General

The TS-PDFT digital function test module provides several groups of digital input and output pins. For this purpose the module has unmultiplexed digital pins, i.e. behind each pin is a separate digital channel. The module also provides variable levels for sensor and driver reference. As a result it is possible to generate suitable logic levels for virtually every application. All settings are made and the clock-pulse is generated on the module itself, so no further stimulus modules are needed.

The usable level range depends on the configuration of the driver references. The driver levels are generated from the CPCI supply (+5 V, +12 V).

If required, all driver pins can be connected to the sensor pins and so stimulate and measure and monitor signal driving. All driver channels can be put into the high-resistance state (TRI-STATE).

The test is time controlled and evaluated locally with a processor. In the

event of a fault, the faulty pins can be identified and reported to the control processor.

NOTE:

The output drivers and input comparators can be set up in 8-bit groups.

5.2 Hardware Description

5.2.1 General

cPCI Interface

A Compact PCI bus (cPCI) interface chip serves as an interface between the PCI bus and the FPGA (Field Programmable Gate Array).

Boot Logic

The boot logic transfers the firmware design of the FPGA from the EEPROM to the FPGA when the module is powered on. This transfer can also be initiated with the software during ongoing operation, thereby making it possible to dynamically adapt the FPGA for future expansions.

FPGA

The FPGA provides the control functions needed to program the analog hardware, digital interfaces and the switching functions.

EEPROM

The EEPROM is used to store the configuration, the correction and the boot data of the FPGA. Access is achieved with the cPCI chip.

Geographical Address Identification

The physical slot number (the GA code of the cPCI chip) is read by the local parallel bus.

5.2.2 Serial Ports

The microprocessor provides serial ports RS232 / K-Bus / SER_xxTTL and CAN.

4th Issue 11.05

5.2.2.1 RS232 / K-Bus

The asynchronous serial port of the microprocessor is used to create an RS232 and K-Bus port and multiplexed on the RS232 or K-Bus transceiver. The microprocessor's RX/TX channels are routed in parallel to the FPGA. A MUX in the FPGA can be used to output these signals as TTL signals on the X10 signals XTO/XTI.

NOTE:

The RS232 port is selected as default.

5.2.2.2 CAN Bus

The microprocessor provides two CAN ports which are directly connected to the CAN transceivers. The first CAN port (CAN1) has a high-speed transceiver, while the second part (CAN2) is equipped with a low-speed, fault-tolerant transceiver. Both ports are routed out on the same CAN bus. The bus can be terminated at one or both ends using 2-pole relays. For CAN voltage level monitoring purposes, the level, buffered by OPs, is made available at the X10 as VCAN_H and V_CANL.

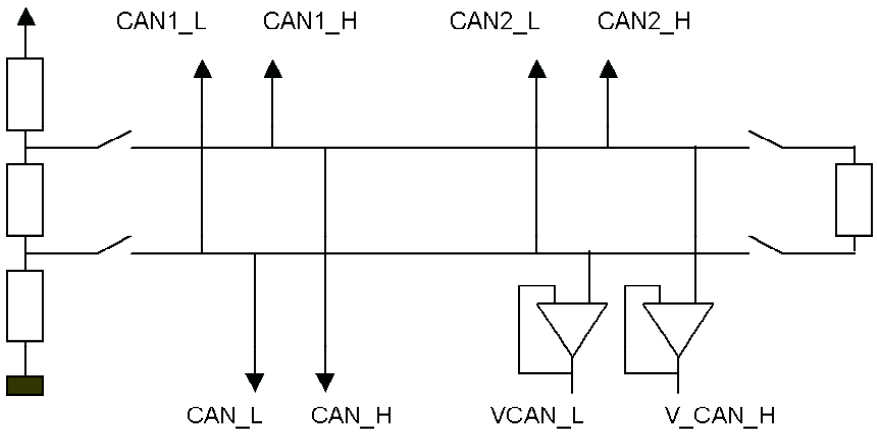

Figure 5-2 CAN Bus

5.2.3 AUX Channels

The AUX channels are connected with 2-pole changeover switches. Each of the signals AUX1..AUX4 is taken from the rear connector X20 (RearIO) to the front connector X10 (3A track each) both directly and via the first relay pole (AUXxA). The pins of the changeover contacts of the second relay poles (AUXxB) are taken out to the X20 and X50 (3A

track each).

5.2.4 Synchronizing

Triggers can be both received and generated to allow synchronizing with other devices, especially with analyzer modules or digital measuring modules. The trigger signals of the PXI trigger bus, the external triggers XTO/XTI on the X10 and two FPGA-internal signals (DINTRIGx) that are derived from two 16-bit pattern comparators of the digital input channels, are available for this purpose. An interrupt for the host processor can be initiated by the DINTRIGx signals and by the microprocessor (data from the microprocessor for the host). The DINTRIGx signals can also initiate an interrupt for the microprocessor or when data have been sent from the host to the microprocessor.

5.2.5 Relay Control

The configuration relays / analog switches are driven by the local SPI interface and the associated shift registers via the microprocessor bus and registers / latches.

5.2.5.1 GND Relay

A switchable GND connection (GND_NO) is needed to be able to run an in-circuit test. This connection is provided by a 2-poles relay.

NOTE:

This connection is open by default.

5.2.6 Digital Output Channels

5.2.6.1 LowPower Output Channels (OUTx)

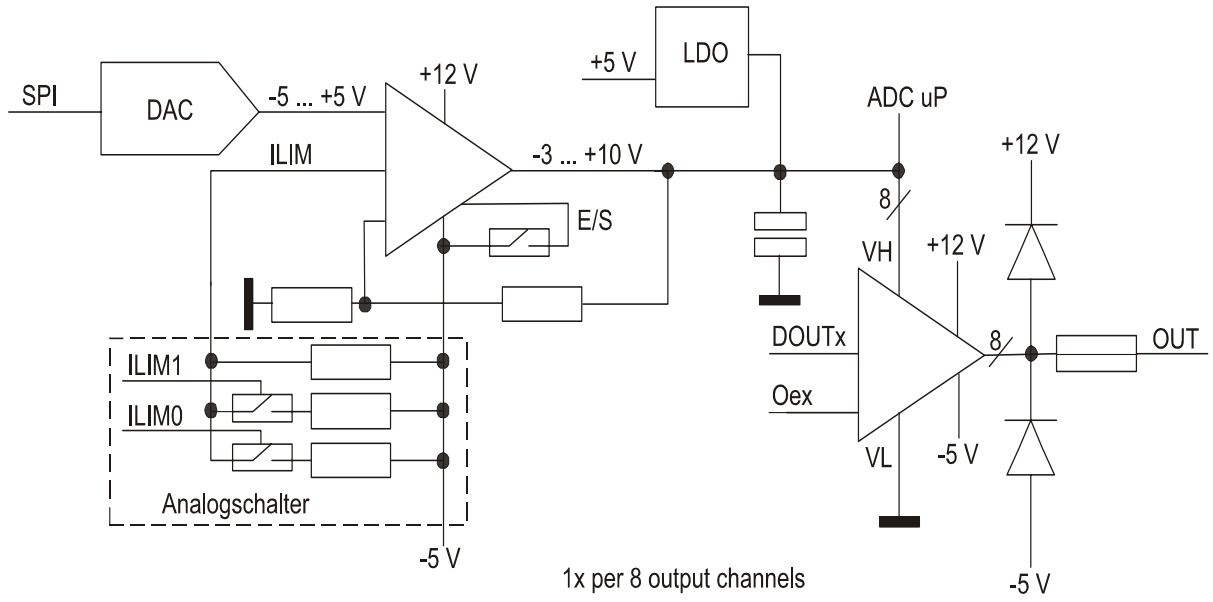

Figure 5-3 Output channel (OUTx)

5.2.6.2 Modes

An individual mode can be selected for each pin group.

- Normal:
  - The output signal is switched to the HIGH supply VH when there is a HIGH at the FPGA output, and to GND with a LOW.
- TRI-State:
  - The output is switched to the high-resistance state whatever the programmed state of the logic (HIGH, LOW).

The mode is selected with the FPGA ports and the programmable FPGA registers. The output registers can be controlled with registers in the FPGA or the stimulus RAM. Programming the stimulus RAM is done with the microprocessor bus, using bits 33 ... 36 for dynamic TRI-STATE control. Microprocessor ports are used to program the TRI-STATE bits.

NOTE:

In the default condition the board's output groups are set for TRI-STATE and microprocessor control.

5.2.6.3 Voltage Levels and Output Current

Each pin group (8 Bit) can be assigned its own programmable HIGH output level. The LOW level is fixed at 0 V. The "HIGH level" of a pin group can be set as a TTL level (3 V) or within the range 0 ... 10 V with a variable output current (0 ... 400 mA). The current output voltage can be read at the ADC ports of the microprocessor.

NOTE:

In the default condition all output groups are programmed for internal supply and TTL levels.

5.2.6.4 Suppressor Circuit

The outputs are permanently protected from short-circuit (multifuse) and the application of back-e.m.f. at the output.

5.2.6.5 HighPower Output Channels (POx)

4 Open Drain driver channels are provided for driving loads with high requirements in terms of voltage and current. These are short-circuit proof and overload resistant. Triggering is parallel from a microprocessor port (PWM outputs). Fault conditions can be read back on the local SPI interface.

5.2.7 Digital Input Signals (INx)

The signals of the digital input channels are compared with programmable reference voltages by analog comparators. The result of this comparison is sent direct to FPGA pins (DINx) and partly in parallel to microprocessor ports.

4th Issue 11.05

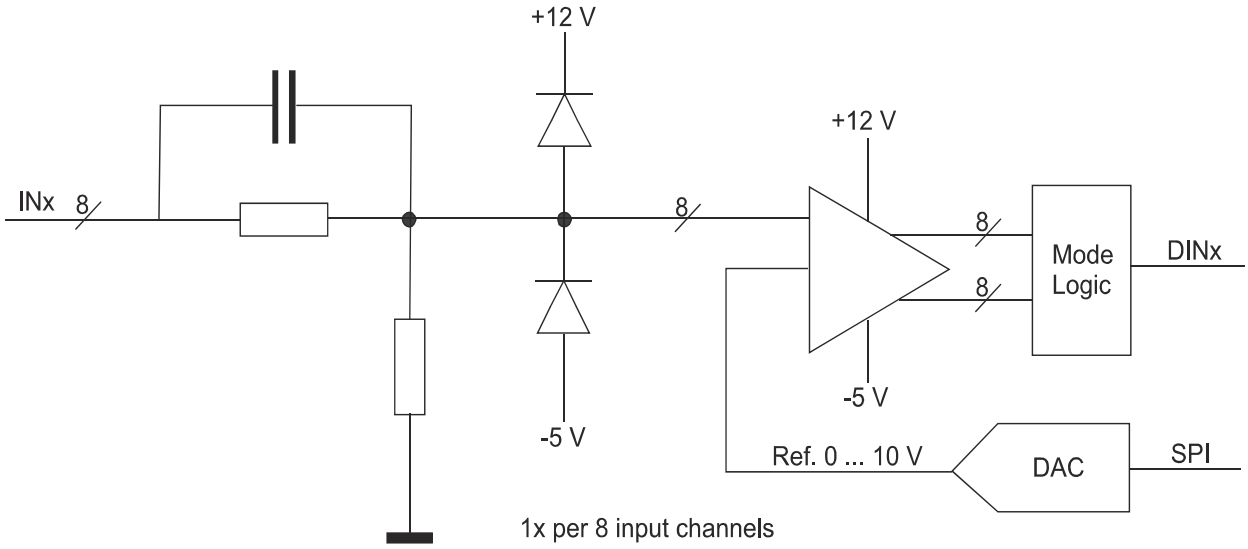

Figure 5-4 Input channel (INx)

5.2.7.1 Modes

The microprocessor can read the status of the input channels with FPGA registers. The mode and the hysteresis of the window comparators can be set for each pin group. If required, measurements can be recorded into the Response RAM (FIFO), controlled by the trigger block. The Response RAM is read over the microprocessor bus.

5.2.7.2 Voltage Levels

The voltage level range without the suppressor circuit responding is -5 V / +12 V. Higher input levels generate higher input currents. An individual threshold of 0 ... +9.5 V can be set by DAC for each pin group (8 bits).

NOTE:

In the default condition the threshold is programmed to the TTL level HIGH = 2.0 V.

5.2.7.3 Suppressor Circuit

Without signal conditioning, the inputs are protected up to ±42 V by a rapid suppressor circuit. The input impedance is reduced from 1 MΩ to 10 kΩ if the circuit becomes active.

5.2.7.4 Bidirectional Pins

All input channels can be connected in groups of 8 to their corresponding output channels by analog switches.

4th Issue 11.05

6 Commissioning

6.1 Installing the TS-PDFT Module

To install the plug-in module, proceed as follows:

- Power down and switch off the CompactTSVP
- Select a suitable front slot (slots 5-15 are possible, best slot 5)
- Remove the corresponding front panel section from the TSVP chassis by slackening the two screws

WARNING!

Check the backplane connectors for bent pins! Any bent pins must be straightened!
Failure to do this may permanently damage the backplane!

- Apply moderate pressure to insert the plug-in module (use locating pin to attach)

WARNING!

To insert the plug-in module, use both hands to guide carefully into the backplane connectors.

- The module is correctly located when a distinct 'stop' can be felt.
- Tighten the two retaining screws on the front panel of the module.

The TS-PDFT module is automatically detected by the CompactTSVP.

4th Issue 11.05

4th Issue 11.05

7 Software

7.1 Driver Software

A LabWindows CVI driver is provided on the card for the PDFT functions. The driver is part of the ROHDE & SCHWARZ GTSL software. All the functions of the driver are described fully in the on-line help and in the LabWindows CVI Function Panels.

The following software modules are installed during driver installation:

Module	Path	Remarks
rspdft.dll	<GTSL Verzeichnis>\Bin	Driver
rspdft.hlp	<GTSL Verzeichnis>\Bin	Help file
rspdft.fp	<GTSL Verzeichnis>\Bin	LabWindows CVI Function Panel File, Function Panels for CVI Development Environment
rspdft.sub	<GTSL Verzeichnis>\Bin	LabWindows CVI Attribute File. This file is needed by some „Function Panels“.
rspdft.lib	<GTSL Verzeichnis>\Bin	Import Library
rspdft.h	<GTSL Verzeichnis>\Include	Header File for the Driver

Table 7-1 Driver InstallationTS-PDFT

NOTE:

The IVI and VISA libraries produced by National Instruments are needed to run the driver.

4th Issue 11.05

7.2 Firmware

The following routines are implemented at firmware level (local processor) and can be activated with commands from the host processor (CompactTSVP).

- Set selected output channels or whole groups
- Interrogate selected output channels or whole groups
- Send and receive routines for the UUT interfaces
- Stimulation, recording and evaluation of digital data streams

7.3 Soft Panel

A soft panel is provided for the module. The soft panel is based on the LabWindows CVI driver and enables the module to be operated interactively. Special test functions can be activated with a protected menu.

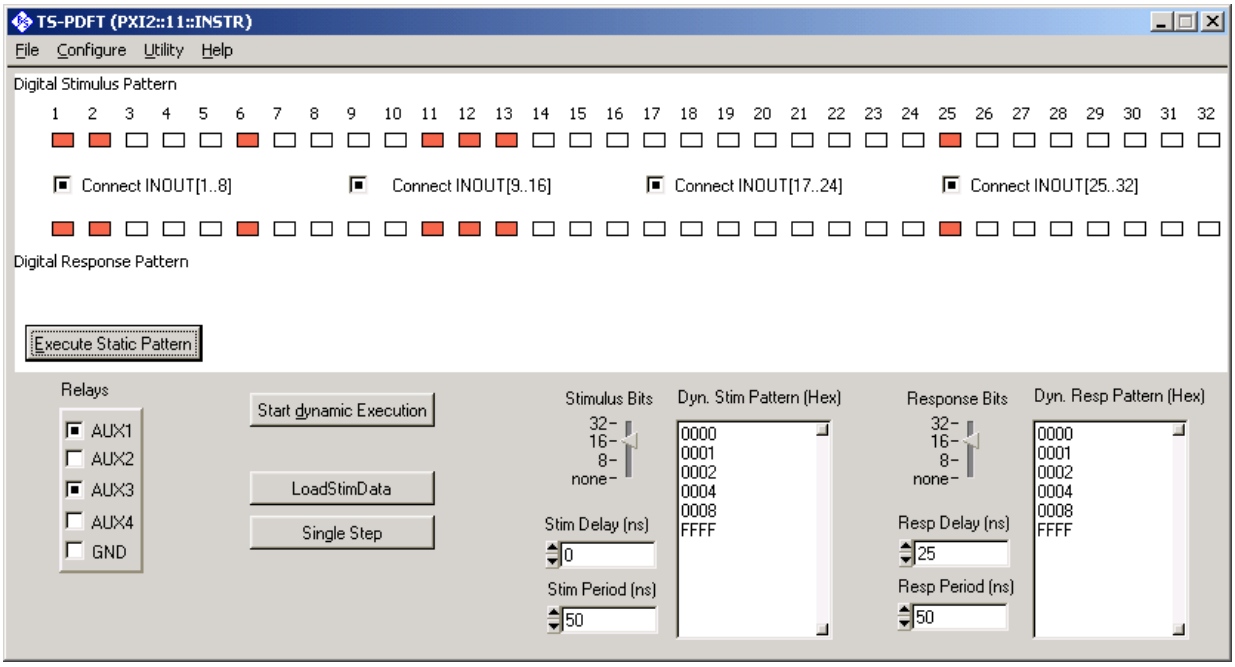

Figure 7-1 Soft PanelTS-PDFT

7.4 TS-PDFT Programming Example

```
/*

    This sample shows the generation of digital functional tests
    using the TS-PDFT module.

    Error handling is not considered in this sample in order to
    keep it easy to read. The return status should be checked for
    VI_SUCCESS after each driver call.

*/

#include "rspdft.h"

/*
    Define channel opcodes with short names (this is easier to read)
*/
#define IOX   RSPDFT_VAL_OPCODE_IOX
#define IL    RSPDFT_VAL_OPCODE_IL
#define IH    RSPDFT_VAL_OPCODE_IH
#define OL    RSPDFT_VAL_OPCODE_OL
#define OH    RSPDFT_VAL_OPCODE_OH

/*
    Sample pattern:

    Stimulus channel out1 generates a clock signal
    Stimulus channel out2 generates a enable signal
    Response channel in1  expects the inverted clock signal
    Response channel in2  expects the direct clock signal if enable=high

    Pattern #  0     1     2     3     4     5     6     7

    Stimulus

               _____       _____       _____       _____
    out1    __|     |_____|     |_____|     |_____|     |__
                              ___________________________
    out2    _____________________|

    Response

               _____       _____       _____       _____
    in1     __|     |_____|     |_____|     |_____|     |__
                              _____       _____       _____
    in2     XXXXXXXXXXXXXXXXXX     |_____|     |_____|
*/

/*
    The following table holds the channel names used:
*/
```

```
#define NUM_CHANNELS_USED 4
static ViChar * s_Channels[NUM_CHANNELS_USED] =
{
  "out1", "out2", "in1", "in2"
};

/*
    The following table describes 8 patterns for the four channels above.
     Note that the opcodes are defined from the unit under test's view,
     i.e. the opcode IL (input low) means that the channel is driven to
     low by a stimulus channel of the TS-PDFT module:
*/
#define NUM_PATTERNS_USED 8
static ViInt32 s_Patterns [NUM_PATTERNS_USED] [NUM_CHANNELS_USED] =
{
/*         out1  out2  in1  in2  */
/* 0 */ {  IL,   IL,   OH,  IOX  },
/* 1 */ {  IH,   IL,   OL,  IOX  },
/* 2 */ {  IL,   IL,   OH,  IOX  },
/* 3 */ {  IH,   IH,   OL,  OH   },
/* 4 */ {  IL,   IH,   OH,  OL   },
/* 5 */ {  IH,   IH,   OL,  OH   },
/* 6 */ {  IL,   IH,   OH,  OL   },
/* 7 */ {  IH,   IH,   OL,  OH   }
};

main ()
{

  ViSession     vi;
  ViStatus      status;
  ViInt32       result;
  ViInt32       patternHandle;
  ViConstString patternSetName = "SamplePattern";
  int           patternIndex;
  int           channelIndex;

  /*
     Open a session to the device driver. The resource descriptor depends
      on the slot number of the TS-PDFT module and must be adapted to the
       target system.
  */

  status = rspdft_InitWithOptions ( "PXI1::11::0::INSTR", VI_TRUE,
VI_TRUE,
                                    "Simulate=0", &vi );
```

```
  /*

=========================================================================
    Configure the channels

=========================================================================
  */

  /*
      Set stimulus ports to 5 V, 100 mA
  */
  status = rspdft_ConfigureStimPort (vi, RSPDFT_MASK_PORT_ALL,
                                     RSPDFT_STIM_MODE_ANALOG, 5.0, 0.1);
  /*
      Set measurement ports to 0.8 ... 2.5 V with hysteresis
  */
  status = rspdft_ConfigureRespPort (vi, RSPDFT_MASK_PORT_ALL,
                                       RSPDFT_RESP_MODE_HYST, 0.8, 2.5);

    /*

=========================================================================
    Static Digital Test

=========================================================================

    The application of stimulus and the collection of responses is done
    at a
    rate controlled by the system controller. Factors such as the amount
    of
    the data, the speed of the controlling CPU and the speed of the
    communication bus determine the rate at which the data is applied to
    the UUT.
  */

  /*
      Configure module for static test and collect all results
  */
  status = rspdft_ConfigureMode (vi, RSPDFT_VAL_EXECUTE_STATIC,
                                     RSPDFT_VAL_COLLECT_ALL);
  /*
      Configure response delay to 10 microseconds
  */
  status = rspdft_ConfigureStaticResponseDelay (vi, 10e-6);
  /*
      Create a pattern
  */
  status = rspdft_CreatePattern (vi, &patternHandle);
```

```
  /*
      Loop over all patterns
  */
  for ( patternIndex = 0; patternIndex < NUM_PATTERNS_USED; patternIndex
  ++ )
  {
    /*
        Configure opcode for all channels
    */
    for ( channelIndex = 0; channelIndex < NUM_CHANNELS_USED;
    channelIndex ++ )
    {
      status = rspdft_ConfigureChannelOpcode (vi, patternHandle,
                                              s_Channels[channelIndex],

s_Patterns[patternIndex][channelIndex]);
    }
    /*
        Execute a single pattern
    */
    status = rspdft_ExecuteStaticPattern (vi, patternHandle);
    /*
        Fetch the result
    */
    status = rspdft_FetchStaticPatternResult (vi, &result);
    if ( result != RSPDFT_VAL_RESULT_PASS )
    {
      /* ... test failed */
    }
  }

  /*
      Free the pattern handle
  */
  status = rspdft_ClearPattern (vi, patternHandle);

  /*

=========================================================================
    Dynamic Digital Test

=========================================================================

    When executing in dynamic mode, the application of stimulus and the
    collection of responses is done at a rate controlled by the
    instrument's timing generator. The channel instructions are stored
   in RAM on the instrument and are applied in parallel under instrument
    control. This allows for greater control over the application rate
    of the data.
  */
```

```
  /*
      Configure module for dynamic test and collect all results
  */
  status = rspdft_ConfigureMode (vi, RSPDFT_VAL_EXECUTE_DYNAMIC,
                                     RSPDFT_VAL_COLLECT_ALL);

  /*
      Create a pattern set
  */
  status = rspdft_CreatePatternSet (vi, patternSetName);
  /*
      Create a pattern
  */
  status = rspdft_CreatePattern (vi, &patternHandle);

  /*
      Start loading the pattern set
  */
  status = rspdft_BeginPatternSetLoading (vi, patternSetName);

  /*
      Loop over all patterns
  */
  for ( patternIndex = 0; patternIndex < NUM_PATTERNS_USED; patternIndex
  ++ )
  {
    /*
        Configure opcode for all channels
    */
    for ( channelIndex = 0; channelIndex < NUM_CHANNELS_USED;
    channelIndex ++ )
    {
      status = rspdft_ConfigureChannelOpcode (vi, patternHandle,
                                              s_Channels[channelIndex],

s_Patterns[patternIndex][channelIndex]);
    }
    /*
        Load the pattern
    */
    status = rspdft_LoadDynamicPattern (vi, patternSetName,
    patternHandle);
  }
  /*
      Pattern set loading is now complete
  */
  status = rspdft_EndPatternSetLoading (vi, patternSetName);
  /*
      Pattern handle is no longer used
  */
  status = rspdft_ClearPattern (vi, patternHandle);
```

```
  /*
     Configure pattern set timing : period = 10 µs, response delay = 5 µs
  */
  status = rspdft_ConfigurePatternSetTiming (vi, patternSetName, 10e-6,
  5e-6);

  /*
      Execute dynamic test
  */
  status = rspdft_ExecutePatternSet (vi, patternSetName, 100);
  /*
      Fetch overall result
  */
  status = rspdft_FetchPatternSetResult (vi, patternSetName, &result);
  if ( result != RSPDFT_VAL_RESULT_PASS )
  {
    /* ... test failed */
  }

  /*
      Free the pattern set
  */
  status = rspdft_ClearPatternSet (vi, patternSetName);

  /*
      Close the session
  */
  status = rspdft_close ( vi );
}
```

8 Self-Test

The TS-PDFT function generator has a built-in self-test capability. The following tests are possible:

- LED Test:
- Power-on test
- TSVP self-test

8.1 LED Test:

When the device is switched on, all three LEDs light up for about one second. This indicates that the 5 V supply is present and all LEDs are working, also that the power-on test was successful. The following statements can be made about the different LED statuses:

LED	Description
One LED does not light up	Hardware problem on the module
No LED's light up	No +5V supply

Table 8-1 Statements about the LED Test

8.2 Power-on test

The power-on test runs at the same time as the LED test. In this test, the result of the FPGA loading process is calculated (FPGA = Field Programmable Gate Array). The following statements can be made about the different statuses of the red and green LEDs:

LED	Description
Green LED on	all supply voltages present
green LED off	at least one supply voltage of the TS-PDFT module is missing
red LED off	no errors were detected
red LED on	FPGA loading failed

Table 8-2 Statements about the power-on test

8.3 TSVP Self-Test

The TSVP self-test runs an in-depth test on the module and generates a detailed log. This is done with the “Self-Test Support Library“.

The TS-PSAM module is used as a measurement unit of R&S modules in the TSVP. The correct operation of the modules is ensured by measurements on the analog bus.

NOTE:

You will find information about starting the self-test and on the sequence of necessary steps in the GTSL software description or the GTSL on-line help.

9 Interface Description

9.1 Connector X10 (Front Connector)

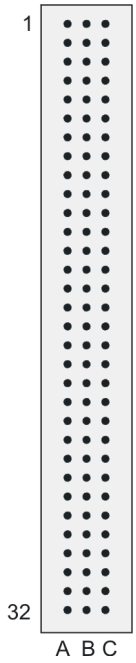

Figure 9-1 Connector X10 (mating side)

Pin	A	B	C
1	AUX1A_NO	AUX1A_COM	PO1
2	AUX2A_NO	AUX2A_COM	PO2
3	AUX3A_NO	AUX3A_COM	PO3
4	AUX4A_NO	AUX4A_COM	PO4
5	OUT1	OUT2	OUT3
6	IN1	IN2	IN3
7	OUT4	OUT5	OUT6
8	IN4	IN5	IN6
9	OUT7	OUT8	**GNDNO**
10	IN7	IN8	**GND**
11	OUT9	OUT10	OUT11
12	IN9	IN10	IN11

Table 9-1 Pin assignment for connector X10

4th Issue 11.05

Pin	A	B	C
13	OUT12	OUT13	OUT14
14	IN12	IN13	IN14
15	OUT15	OUT16	**GNDNO**
16	IN15	IN16	**GND**
17	OUT17	OUT18	OUT19
18	IN17	IN18	IN19
19	OUT20	OUT21	OUT22
20	IN20	IN21	IN22
21	OUT23	OUT24	**GNDNO**
22	IN23	IN24	**GND**
23	OUT25	OUT26	OUT27
24	IN25	IN26	IN27
25	OUT28	OUT29	OUT30
26	IN28	IN29	IN30
27	OUT31	OUT32	**GNDNO**
28	IN31	IN32	**GND**
29	XTO	RS232_TX	KBUS_L
30	XTI	RS232_RX	KBUS_H
31	CAN_L	VCAN_L	**GND**
32	CAN_H	VCAN_H	**CHA-GND***

Table 9-1 Pin assignment for connector X10

* = Signal **CHA-GND** is connected to the front panel of the TS-PDFT .
The front panel is capacitively coupled to GND.

4th Issue 11.05

9.2 Connector X20 (Extension Connector)

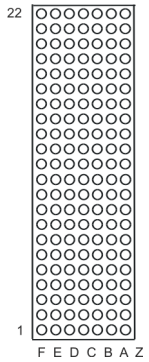

Figure 9-2 Connector X20 (mating side)

Pin	F	E	D	C	B	A	Z	
22		GA0	GA1	GA2	GA3	GA4		
21		OD8						
20		+5V	GND	+5V	AUX1A_COM	AUX2A_COM		
19		AUX1A_COM	AUX2A_COM	+5V	GND	-12V		
18		PXI_TRIG6	GND	PXI_TRIG5	PXI_TRIG4	PXI_TRIG3		J20
17		PXI_CLK10	PO_2	PO_1	GND	PXI_TRIG2		
16		PXI_TRIG7	GND	PO_3	PXI_TRIG0	PXI_TRIG1		
15			+5V	PO_4	GND			
14	NC	AUX1A_NC	AUX1A_NO		AUX3A_NO	AUX3A_NC	NC	C
13	NC	AUX1A_NC	AUX1A_NO		AUX3A_NO	AUX3A_NC	NC	O
12	NP	AUX1A_COM	AUX2A_NO		AUX4A_NO	AUX3A_COM	NP	N
11	NP	AUX1A_COM	AUX2A_NO	IL1	AUX4A_NO	AUX3A_COM	NP	N
10	NC	AUX2A_COM	AUX2A_NC		AUX4A_NC	AUX4A_COM	NC	E
9	NC	AUX2A_COM	AUX2A_NC		AUX4A_NC	AUX4A_COM	NC	C
8	NC	AUX1B_COM	AUX1B_NO		AUX3B_NC	AUX3B_COM	NC	T
7	NC	AUX1B_COM	AUX1B_NC	IL2	AUX3B_NO	AUX3B_COM	NC	O
6	NC	AUX2B_COM	AUX2B_NO		AUX4B_NC	AUX4B_COM	NC	R
5	NC	AUX2B_COM	AUX2B_NC		AUX4B_NO	AUX4B_COM	NC	
4	NC						NC	
3		RSA0	RRST#		GND	RSDO		
2		+12V	RSDI	RSA1		RSCLK		
1		+5V			GND	RCS#		

Table 9-2 Pin assignment for connector X20

9.3 Connector X1 (cPCI Bus Connector)

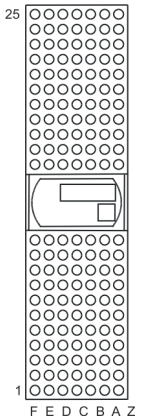

Figure 9-3 Connector X1 (mating side)

Pin	F	E	D	C	B	A	Z	
25	GND	5V	3.3V	ENUM#	REQ64#	5V	GND	
24	GND	ACK64#	AD[0]	V(I/O)	5V	AD[1]	GND	
23	GND	AD[2]	5V	AD[3]	AD[4]	3.3V	GND	
22	GND	AD[5]	AD[6]	3.3V	GND	AD[7]	GND	
21	GND	C/BE[0]#	M66EN	AD[8]	AD[9]	3.3V	GND	
20	GND	AD[10]	AD[11]	V(I/O)	GND	AD[12]	GND	X1
19	GND	AD[13]	GND	AD[14]	AD[15]	3.3V	GND	
18	GND	C/BE[1]#	PAR	3.3V	GND	SERR#	GND	
17	GND	PERR#	GND	IPMB_SDA	IPMB_SCL	3.3V	GND	C
16	GND	LOCK#	STOP#	V(I/O)	GND	DEVSEL#	GND	O
15	GND	TRDY#	BD_SEL#	IRDY#	FRAME#	3.3V	GND	N
12..14				Key Area				N
11	GND	C/BE[2]#	GND	AD[16]	AD[17]	AD[18]	GND	E
10	GND	AD[19]	AD[20]	3.3V	GND	AD[21]	GND	C
9	GND	AD[22]	GND	AD[23]	IDSEL	C/BE[3]#	GND	T
8	GND	AD[24]	AD[25]	V(I/O)	GND	AD[26]	GND	O
7	GND	AD[27]	GND	AD[28]	AD[29]	AD[30]	GND	R
6	GND	AD[31]	CLK	3.3V	GND	REQ#	GND	
5	GND	GNT#	GND	RST#	BSRSV	BSRSV	GND	
4	GND	INTS	INTP	V(I/O)	HEALTHY#	IPMB_PWR	GND	
3	GND	INTD#	5V	INTC#	INTB#	INTA#	GND	
2	GND	TDI	TDO	TMS	5V	TCK	GND	
1	GND	5V	+12V	TRST#	-12V	5V	GND	

Table 9-3 Pin assignment for connector X1

9.4 Connector X50 (optional push-on module)

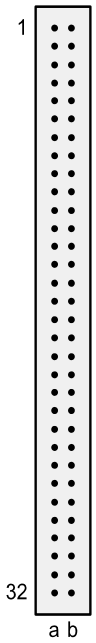

Figure 9-4 Connector X50 (mating side)

Pin	a	b
1	GNDNO_1	GNDNO_0
2	AUX4A_NC	AUX4B_NC
3	AUX4B_COM	GND
4	-12V	AUX4A_COM
5	AUX4A_NO	AUX4B_NO
6	AUX3A_NC	AUX3B_NC
7	AUX3B_COM	GND
8	+12V	AUX3A_COM
9	AUX3A_NO	AUX3B_NO
10	AUX2A_NC	AUX2B_NC
11	AUX2B_COM	GND
12	+5V	AUX2A_COM
13	AUX2A_NO	AUX2B_NO
14	AUX1A_NC	AUX1B_NC

Table 9-4 Pin assignment of connector X50

Pin	a	b
15	AUX1B_COM	GND
16	+3.3V	AUX1A_COM
17	AUX1A_NO	AUX1B_NO
18	PO1	PO2
19	PO3	PO4
20	SPI_A0	SPI_A1
21	SPI_CLK	SPI_DOUT
22	SPI_CS_X50	SPI_DIN
23	nRESET	BID_X50
24	OD5	OD6
25	40MHz	OD7
26		
27	GND	GND_X30
28	IL1	IL2
29	ABA1	ABC1
30	ABC2	ABB1
31	ABA2	ABB2
32	ABD1	ABD2

Table 9-4 Pin assignment of connector X50

10 Specifications

NOTE:

In the event of any discrepancies between data in this manual and the technical data in the data sheet, the data sheet takes precedence.

10.1 Scope of Application

Digital function tests:	High-Speed
Digital function tests:	Low-Speed
Plug-in module for use in:	ROHDE & SCHWARZ CompactTSVP
Space required in the CompactTSVP:	1 Slot at the front
Interface:	CPCI interface (PICMG 2.0 Rev. 2.1) for 5 V backplane

10.2 Input/output channels

10.2.1 Data Output Channels

Number of channels:	32, in 4 groups, short-circuit proof
Modes per group*:	TRI-State, TTL, analog
Output level TTL*: Output level analog*:	3.3 V -3 ... 10 V, 12 bit resolution
Output current per channel: Output current per group:	max. 150 mA max. 700 mA
Output rate:	Static, 40 MS/s
Protection:	Output current (analog), selectable by group

4th Issue 11.05

Real-time data storage:	131071 Sample x 8 Bit or 65535 Sample x 16 Bit or 32768 Sample x 32Bit

(* = can be selected by group)

10.2.2 Data Input Channels

Number of channels:	32, in 4 groups
Modes per 2 groups:	Hysteresis, window comparator
Input level*: threshold 1*: threshold 2*:	-5 ... 12 V 0 ... 9.5 V 0 ... 9.5 V
Hysteresis*:	programmable, threshold 1,2
Input impedance:	1 MΩ
Protection:	Overvoltage protection ±42 V
Real-time data storage:	131071 Sample x 8 Bit or 65535 Sample x 16 Bit or 32768 Sample x 32Bit

(* = can be selected by group)

10.2.3 Power Output Channels

Number of channels:	4, Low-Side FET drivers
Level range:	0 ... 45V
Max. output current:	max. -1 A
Max. output frequency	40 kHz, pulse-width modulated
Protection:	long-term short-circuit proof

4th Issue 11.05

10.2.4 Relay Channels

Number of channels:	5x (AUX 1...4, 1x GND_NO)
Max. switching capacity	60 VDC / 1.5 A / 100 W

10.3 Control Logic

10.3.1 Local Control Logic

Microprocessor:	ST10, 16 bit, 40 MHz, 2 MB RAM
Ports:	1x CAN High/Low Speed 1x RS232 / K-Bus

10.3.2 Synchronization

Trigger inputs:	1x local TTL trigger 8x PXI trigger bus 4x pattern comparator inputs
Edge:	Positive / negative edge
Pattern:	13 bit, 3 states: • High • Low • don’t care
Delay:	40ns ... 100s
Trigger Outputs:	1x local TTL trigger, 8x PXI trigger bus

10.3.3 Reference Clock

PXI Clock:	10 MHz

10.3.4 Primary Connection

Inputs with outputs:	programmable, in 4 groups

4th Issue 11.05

10.4 General Data

Power consumption:	3.3 V / 0.5 A, +5 V / 1.6 A, +12 V / 0.2 ... 2.4 A, -12 V / 0.1 A
EMC:	according to EMC Directive 89/336/EEC and Standard EN61326
Safety:	CE, EN61010 Part 1
Mechanical strength	
• Vibration test sinusoidal Sine 5 Hz ... 55 Hz: Sine 55 Hz ... 150 Hz:	 2 g, MIL-T-28800D, class 5 0.5 g, MIL-T-28800D, class 5
• Vibration test random 10 Hz ... 300 Hz:	 1.2 g
Shock test:	40 g, MIL-STD-810. Classes 3 and 5
Temperature load	
• Nominal temperature range:	+5 ... +40 °C
• Operating temperature range:	+0 ... +50 °C
• Storage temperature range:	-40 ... +70 °C
• Humidity:	+40°C, 95% RH
Dimensions in mm:	316 x 174 x 20
Weight:	0.37 kg
Calibration interval (recommended):	1 year

10.5 Ordering Information

Digital Function Test Module TS-PDFT	1143.0080.02
Platform, TS-PCA3	1152.2518.02

4th Issue 11.05